FLEXlogic™ iFX780 Third Party Tool Support

Company & Product	Product Description	Company Address & Phone	PLD Version & FPGA Support Target Dates
Acugen ATGEN™ Test Generation Software	Automatically generates high coverage functional test vectors for all types of programmable logical devices. These test vectors can be applied after programming either on the programmer, a device tester, or during circuit testing. • Event driven time-based simulator, concurrent fault simulation. • Devices supported: PAL, PLDs, and FPGAs. • Testers supported: Sentry, GenRad, Teradyne, HP, & others. • MS-DOS, DEC VAX/VMS, Sun-3, & Sun-4.	427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	PLD SUPPORT: v2.51 FPGA: 1H, 1993
Cadence Composer™	A comprehensive suite of design entry, debug, and documentation capabilities. • Top-down, mixed-level design allows creation of hierarchial schematics mixed with textual design descriptions. • Advanced editing capabilities minimize tedious entry tasks, freeig time for design analysis. • Sophisticated, on-line rule checks for detecting design errors. • Integration provides a thigly-coupled solution, binding together leading applications for analysis, synthesis, layout, and documentation. PLD support is also available through integration of Data I/O and Minc PLD tools.	555 River Oaks Parkway, Bldg. 1 San Jose, CA 95134 (408) 943-1234	FPGA: April, 1993
Verilog-XL™ & VHDL-XL™	Digital logic simulators provide advanced simulation capabilities to handle complex electronic designs. • High-performance simulation meets difficult deisgn challenges. • Mixed-level simulation. • Complete interactive debug environment. • Accurate modeling and extensive library support. • Open design environment.		FPGA: April, 1993
Data I/O ABEL™ -4	Design software lets you describe and implement logic designs using behavioral language and can be simulated and converted into JEDEC Standard format. • Devices supported: PLD, FPGA, & PROM. • Entry methods: ABEL, Truth Table, State Machine, and Boolean Equation. • MS-DOS, Sun-3, SunSPARC, DEC VAX/VMS, Apollo(TM)	10525 Willows Road, N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	PLD SUPPORT: DOS/Sun v4.2 Apollo v4.1 VMS v4.0 FPGA: March, 1993
PLDtest® Plus	An integrated software package that combines a testability analysis of the device under design or test with fault grading and automatic test vector generation (ATVG). • MS-DOS, DEC VAX/VMS v5.0, Sun-3, and SunSPARC stations.		PLD SUPPORT: v2.1 FPGA: April, 1993

Data I/O 2900	Device Programmer • RS232C port connection to the PC. • Devices supported: DIP, PGA, PLCC, SOIC, & LCC. • Can program almost all PLDs and memory devices. • Testing: Functional, Parallel test vector, and device continuity.	10525 Willows Road, N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	PLD SUPPORT: v1.3 FPGA: Q1, 1993
Unisite™	Device Programmer • RS232C port connection to the PC. • Devices supported: DIP, PGA, PLCC, SOIC, & LCC. • Can program almost all PLDs, memory devices, and microcontrollers. • File types supported: JEDEC, Intel Hex-32, and many others.		PLD SUPPORT: v1.9 FPGA: Q1, 1993
Logic Modeling SmartModel Library	Combines the benefits of behavorial models, including fast simulation and minimum storage requirements, with structural level accuracy. • Behavorial models for high-performance simulation • Accurate modeling of device functionality and timing • Intelligent handling of unknown conditions Simulators supported: • AT&T, DAZIX/Intergraph, Mentor Graphics, Valid Logic Systems, ViewLogic Systems, Cadence Design Systems, Genrad, Racal-Redac, and Vantage Analysis Systems Platforms supported: • Data General, HP/Apollo, Intergraph, Sun Microsystems, Digital Equipment Corporation, IBM, and Sony	19500 N.W. Gibbs Drive P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	FPGA: Jan, 1993
Logical Devices CUPL™	A high level, universal design software package for PLDs and FPGAs. It offers a: • Variety of design expression formats • True language flexability • DeMorgan expansion • Simulation • Output: JEDEC Format	1201 N.W. 65th Place Ft. Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	PLD SUPPORT: v4.2A FPGA: Feb, 1993
ALLPRO™	Universal device programmer. • Bus card interface for PC. RS232 connection for all other computers. • Devices supported: DIP, PGA, PLCC, SOIC, & LCC device packages. • Testing: functional, diagnostic, internal logic, and others. • File types: JEDEC, Intel hex 80 & 86, and others.		PLD SUPPORT: v2.1 FPGA: Q1, 1993
Mentor Graphics Design Architect	An integrated system of schematic, symbol, and text editors for capturing designs. Including • Schematic capture • VHDL description • Automatic net routing • Interwindow editing • HP/Apollo-Mentor workstations	8005 S.W. Boeckman Road Wilsonville, OR 97070-7777 (503) 685-7000	FPGA: Feb, 1993
Idea Station	Includes the company's Design Architect design creation tools, a System 1076 VHDL editor, and the QuickSim II high-performance logic simulator. An additional option of the Idea Station is the Autologic family of logic synthesis tools, which help put a complete, top-down design methodology into every designer's hands.		FPGA: Feb, 1993

Mentor Graphics Autologic	Autologic family of logic synthesis tools, which help put a complete, top-down design methodology into every designer's hands.	8005 S.W. Boeckman Road Wilsonville, OR 97070-7777 (503) 685-7000	FPGA: 1H, 1993
Quicksim II & Simview	High performance logic simulator for function & performance verification of FPGAs, large ASICs and complex circuit boards. QuickSim II supports a complete hierarchy of modeling methods, including gate and table primitives, behavioral, VHDL and hardware based models.		FPGA: 1H, 1993
Minc PLDesigner PLDesigner-XL	A powerful design tool that can be used for all types of programmable logic including PLDs, CPLDs, and FPGAs. • Automatic device selection based on user-specified design criteria. • Automatic partitioning across multiple PLDs. • Quick, easy retargeting between FPGA and PLD. • Functional simulation. • Import from high-level language, waveform deitor, or schematic import.	6755 Earl Drive Colorado Springs, CO 80918 (719) 590-1155	PLD SUPPORT: v4.2 FPGA: 1H, 1993
OrCAD PLD Tools	Software tool for programming PLDs. JEDEC Format output. • Schematic entry from OrCAD SDT. • Test vector generation. • 7 forms of input include Boolean equations, State Machines, Truth Tables • MS-DOS, Sun	3175 N.W. Aloclek Drive Hillsboro, OR 97124 (503) 690-9881	PLD SUPPORT: v1.0.3 FPGA: Feb, 1993
Schematic Design Tool	Graphical environment for electrical design projects. • Import/export to PSpice, OrCAD/PLD, OrCAD/VST • Netlist conversion into 30 different formats including Intel ADF. • MS-DOS, Sun		FPGA: Feb, 1993
Verification, Simulation Tool	A series of software tools for performing timing-based simulation of digital designs. • Includes component modeling program. • Accepts OrCAD/SDT generated netlists. • MS-DOS, Sun		FPGA: Feb, 1993
Viewlogic WorkView & PowerView	Integrated schematic capture and simulation environment • Entry methods: VHDL, Schematic, ABEL, JEDEC, State Mach., Truth Table, Logic Equations. • Automatically partitioning and optimization into PLD architecture. • full timing/fault simulation. • IBM PC - WorkView • UNIX - PowerView	2350 Mission College Blvd., Suite 1000 Santa Clara, CA 95054 (408) 982-3881	PLD SUPPORT: Workview v4.1 FPGA: Feb, 1993